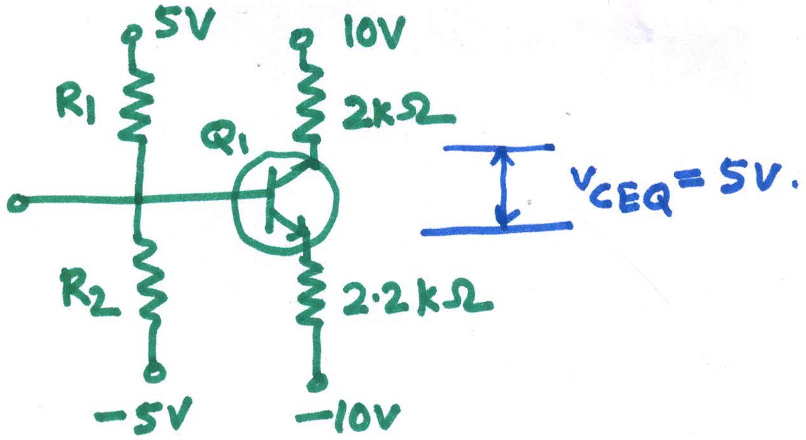
Solutions of Quiz - II

Basic ECE Q.

RAKTIM HALDAR.

Q.1.



for stability.

$R_{TH} = \frac{1}{10}(1+\beta)R_E$

$= 13.42\ k\Omega$

Options (b), (c), (d) satisfy this.

Eliminate (a).

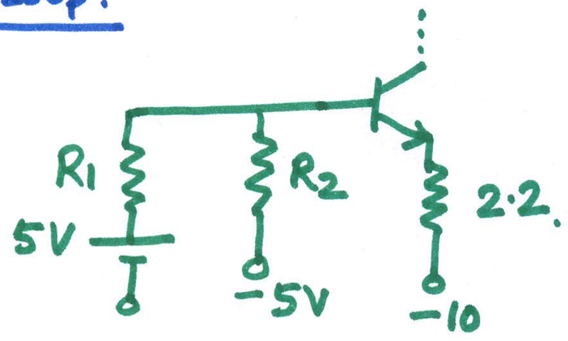
Now, find I_E, I_c.

from KVL → $10 - 2I_c - 5 - 2.2I_E - (-10) = 0$

$\Rightarrow 10 - 2\beta I_B - 5 - 2.2(1+\beta)I_B + 10 = 0$.

$\therefore I_B = 0.06\ mA$.

I/P Loop:



$V_{TH} = \frac{10R_2}{R_1+R_2} - 5$

$R_{TH} = 13.42k\Omega = \frac{R_1R_2}{R_1+R_2}$

Now, $I_B = \frac{V_{TH} - 0.7 - (-10)}{R_{TH} + (1+\beta)R_E} = 0.06$

$\therefore V_{TH} = -0.4428$.

$$\therefore \frac{10R_2}{R_1+R_2} = 0.4428 + 5 = 4.5572\text{V}$$

$$\therefore \frac{10R_2}{R_1+R_2} = 4.5572. \quad \text{—(I)} \qquad \frac{R_1R_2}{R_1+R_2} = 13.42 \quad \text{—(II)}$$

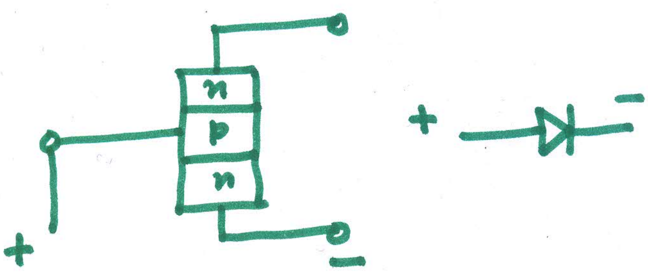
Dividing (I)/(II) →

$$\frac{10R_2}{R_1+R_2} \times \frac{R_1+R_2}{R_1R_2} = 0.3388$$

$$\therefore R_1 \cong 29.45\ \text{k}\Omega$$
$$R_2 \approx 24.66\ \text{k}\Omega.$$

[Ans. (c)]

Q.2.



forward bias.
Low resistance.

Ans. (c)

Q.3.

$$V_{TH} = \frac{20R_2}{R_1+R_2} = 3.7\text{V}, \qquad R_{TH} = 4.074\ \text{k}\Omega.$$

$$\therefore I_B = \frac{V_{TH} - 0.7}{R_{TH} + (1+\beta)R_E} = 0.05497\ \text{mA} \approx 0.06\ \text{mA}$$

$$\therefore I_E = (1+\beta)I_B = 5.55\ \text{mA} \approx 6\ \text{mA}.$$

Ans: (d)

4. a_0  A ≡ OPAMP → VCVS **(Ans: (a))**

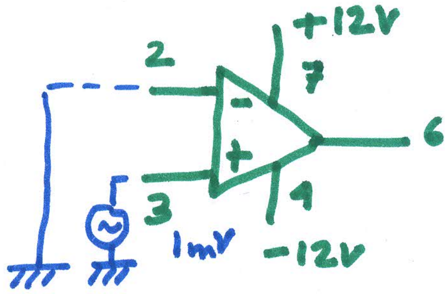
Voltage $\xrightarrow{G}$ Voltage

G → HIGH Gain.

5. $G = \left(1 + \frac{R_2}{R_1}\right) > 1$ **(b) Greater than one.**

6. **(d) Inverting**

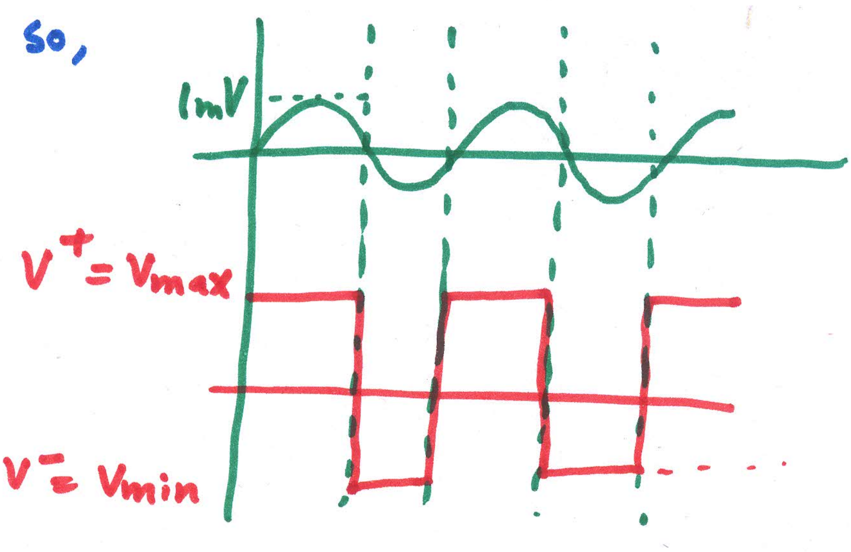
7. This one is really a tricky and beautiful Q.



The gain (open-loop) is very high, ideally → ∞

But the dc bias provides maximum of 12V. So the o/p cannot be more than this (ofcourse not infinite). The OPAMP will saturate before this.

So,



← Applied to the non-inverting terminal (+)

So, —

Ans. (b) square wave

8. Read OPAMP frequency response.

The gain-bandwidth product for an OPAMP will be constant.

$\therefore \; G \times BW = C$

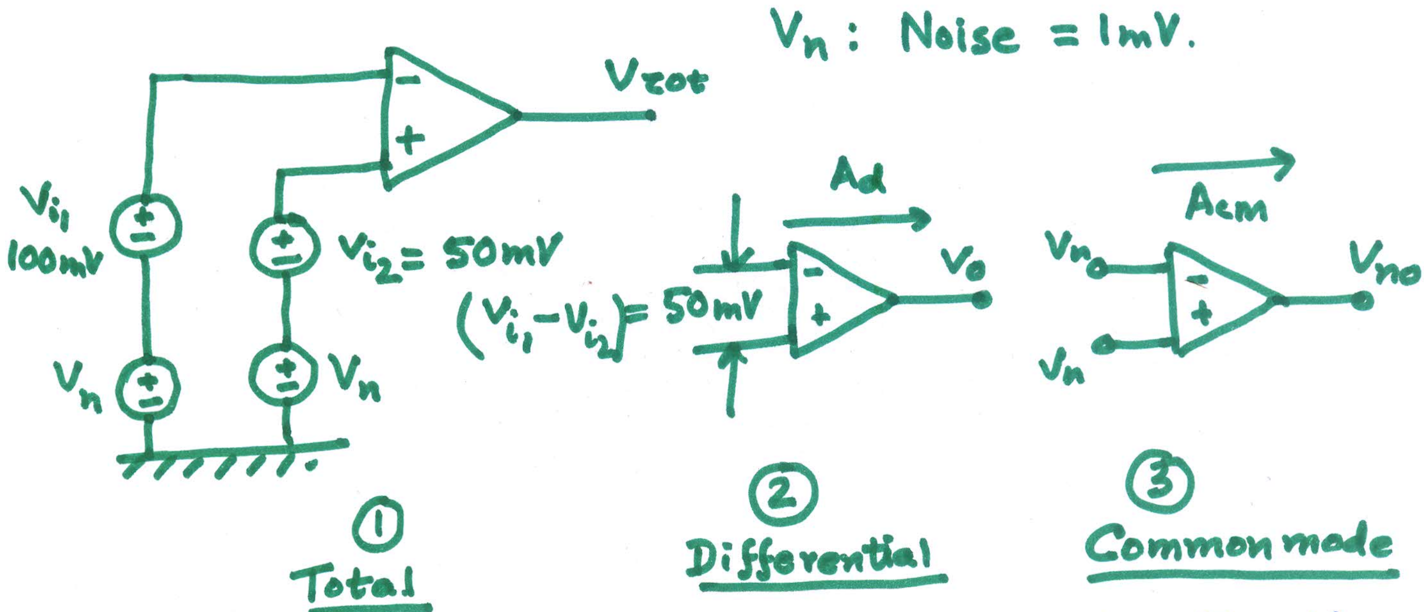
$\therefore \; 1 \times 1.5 \times 10^6 = 100{,}000 \times f_c$

$\therefore \; f_c = 15\,Hz.$ **Ans. (c) 15 Hz.**

9. $CMRR = 20 \log_{10} \frac{A_d}{A_{CM}} = 90.$ **Ans: (d)**

$A_d = 150$

$\therefore \; A_{CM} \cong 4.7 \times 10^{-3}.$



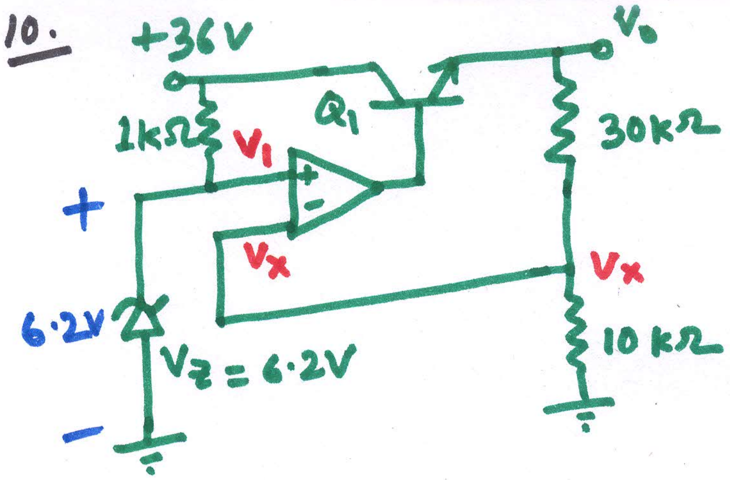
$\therefore$ Differential Voltage $= V_{i_1} - V_{i_2} = V_d = 50\,mV.$

$\therefore$ O/P Signal $= V_o = A_d V_d = 150 \times 50 = \underline{7.5\,V}$ I

Common Voltage = Noise $= V_n = 1\,mV.$

$\therefore$ O/P Noise $= V_{no} = A_{CM} \cdot V_n = \underline{4.7 \times 10^{-6}\,V.}$ II

10.



$V_1 = 6.2V$

One can check that the Zener diode would be ON by open-circuit the Zener diode.

So, if the OPAMP is ideal.

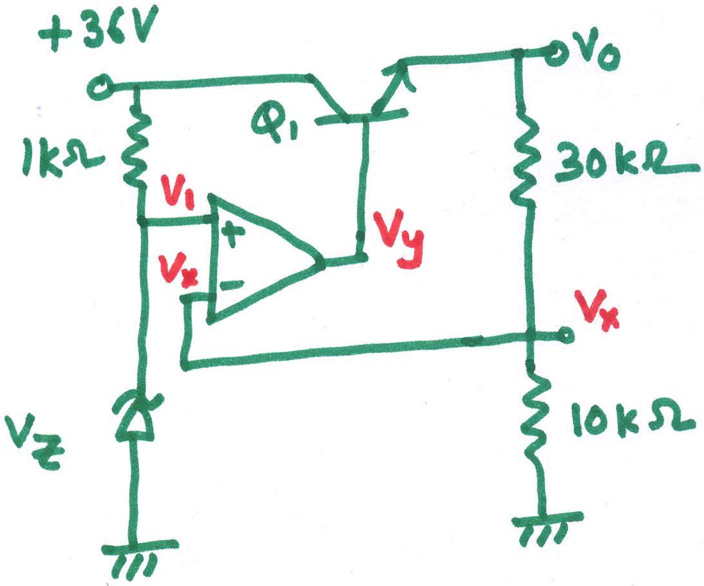
$V_x \approx V_1 = 6.2V.$

$$\therefore \quad V_x = \frac{V_o \times 10}{30+10} \quad \text{(voltage divider).}$$

$$\therefore \quad V_o = 6.2 \times 4 = 24.8\ V.$$ **[Ans. (b)]**

11. One can guess the ans will be 24.7V

procedure →



$V_1 = 6.2V$

$V_x \neq V_1$ (as the OPAMP is not ideal now).

Rather,

$V_y = (V_1 - V_x) \times 1000.$

now, $V_o = (V_y - 0.7V)$

again $V_x = \frac{V_o \times 10}{40}$

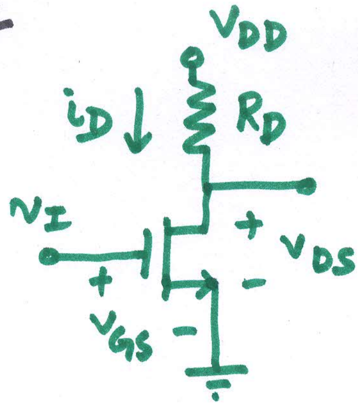
$\therefore \quad V_o = 4V_x.$

$\therefore \quad (V_1 - V_x) \times 1000 - 0.7 = V_o = 4V_x.$

Solve this, you will eventually get, V_x, V_o both.

Ans: (a) 24.7V

13.



The MOSFET is biased in the non-saturation region.

$i_D = K_n [2(v_I - V_{TN}) v_o - v_o^2]$

$v_o = V_{DD} - i_D R_D.$

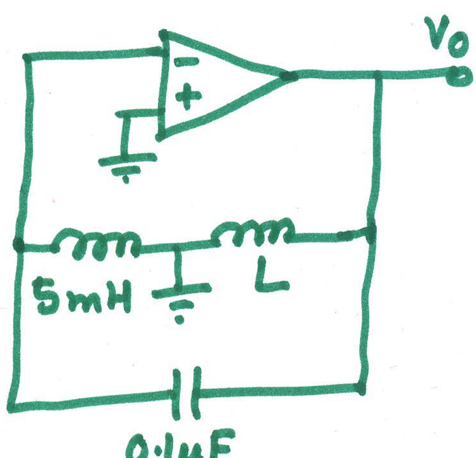
$P = v_o \times i_D$

$\therefore v_o = 0.2V, \; v_i = 5V, \; v_{TN} = 1V, \; R_D = 500\Omega.$

$\therefore K_n = 6.15 \; mA/V^2.$ and $P = 1.92 \; mW$

Ans: (b) 1.92 mW.

14.



$$f = \frac{1}{2\pi\sqrt{L_{eq}C}}$$

$$L_{eq} = \frac{1}{4\pi^2 f^2 C} = 101 \; mH.$$

$$L_{eq} = L + 5 \; mH.$$

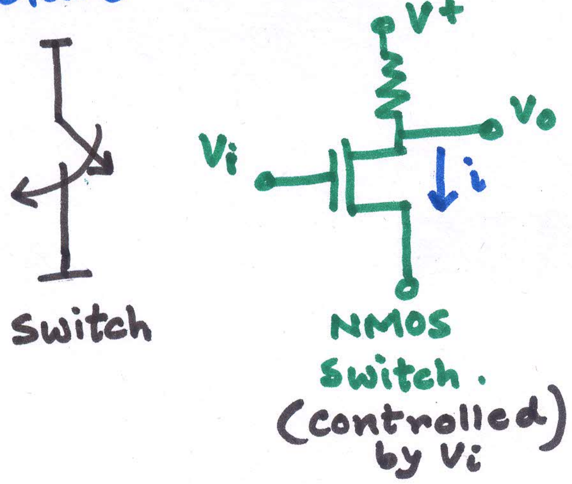
$$\therefore L \cong 96 \; mH. \cong 96.3 \; mH$$

Ans: (C) 96.3 mH.

This is probably the 'Hartley Oscillator' configuration with OPAMP. Please confirm if it is included in the syllabus or not.

15.

Gate as a switch: Controlled switch

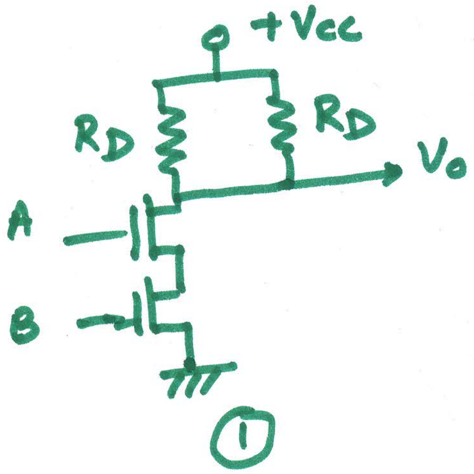


1. If V_i = 5V (ON)/HIGH (logical 1)
2. then current will flow through NMOS
3. SO, NMOS → ON or short-circuited with GRD.
4. So, if $V_i = 1$ (5V) → NMOS ON → SHORT with Ground, → $V_o = 0$ (0V)
5. NMOS → NOT GATE.

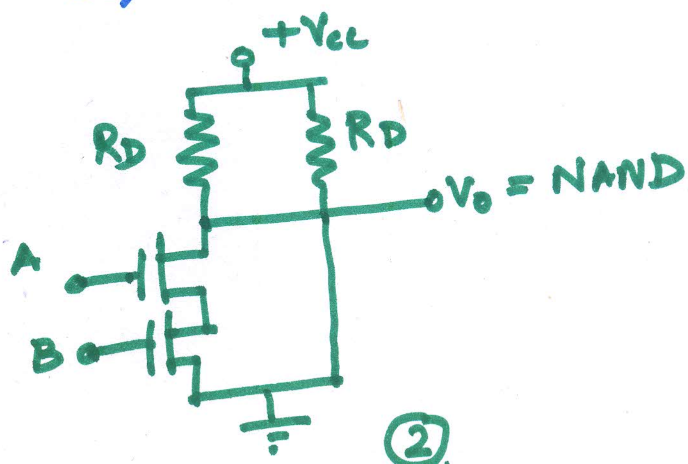
So, for this problem,—

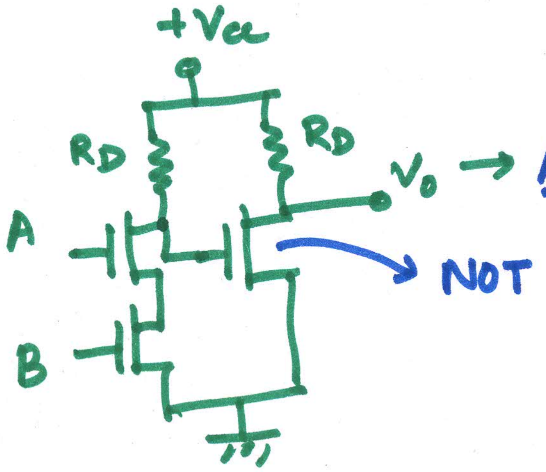
If Both A, B = 1 then $V_o = 0$

∴ NAND.



So, if





V_o → <u>AND</u> (Extra NOT is there)

∴ NAND + NOT = AND.

Ans: (a) AND.